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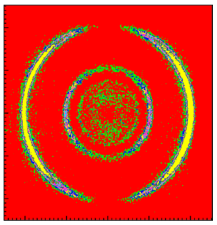
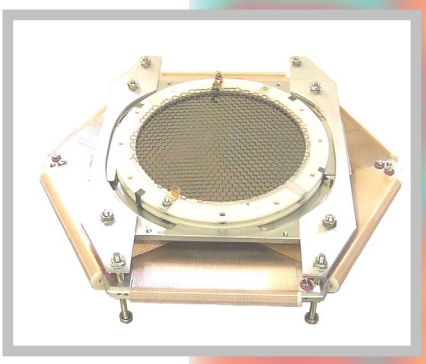
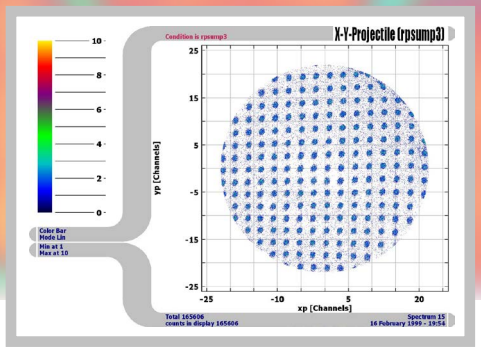


The ATR19-8/6/2 amplifier&timing-discriminator modules

(Version 11.0.2402.1)





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3 The ATR19 Amplifier & CFD Module

The readout of the MCP and delay-line anode signals requires amplifying and precise timing (discrimination) circuits such as "Constant-Fraction Discriminators" (CFD). Those produce digital signals (like NIM or ECL) for a follow-up time measuring device, e.g. a time-to-digital converter (TDC).

The **ATR19** modules were especially designed for this timing detector read out purpose. Its common version nowadays is the **ATR19-2b**, see Chapter 3.6. In the version as 1 HU 19" case with internal mains power supply it can host up to four **DLATR** differential timing amplifier & CFD boards, each with two independent channels. It provides all input/output connectors, level controls and a 100-125 V/200-250 V AC power adapter. The module is typically delivered either with 3 boards (**ATR19-6**, 6 channels total), for use with the **DLD** detectors or with all slots occupied (**ATR19-8**, 8 channels total) e.g. for use with **Hex**-detectors. Each version can either provide the timing signals as NIM or differential ECL level, e.g. depending on the requirements of the time measuring device. The **ATR19-2b** module version as 3 HU cassette hosts only one board and contains the same input/output options as the larger unit and comes with an external mains adapter*. Only the older **ATR19-2** model requires a mains power adapter with ±6 V (<0.5 A) for operation, such as the **RoentDek SPS1(b)**. Its circuits are similar to the internal supply in the **ATR19-6/8** and can also be used as a back-up external mains adapter for those units, and also for earlier **(N)DLATR6/8** models.

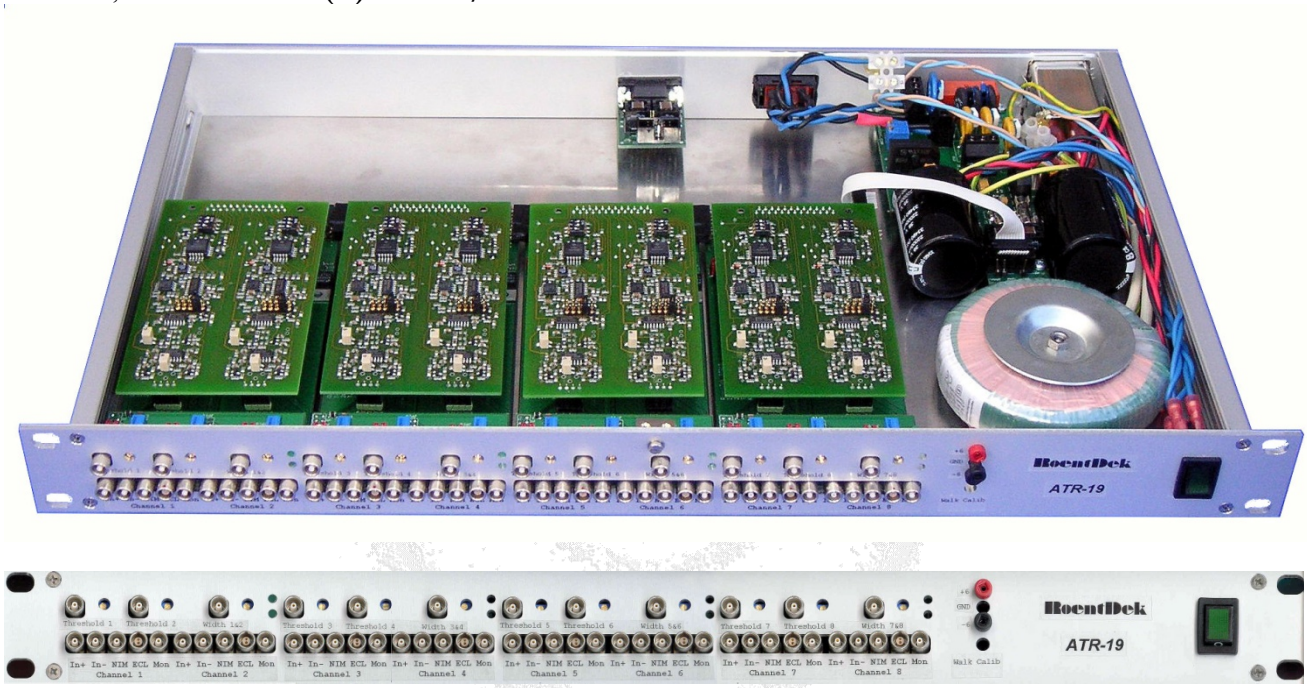


Figure 3.1: The ATR19 module (here ATR19-8)

The differential amplifying stage of the internal **DLATR**-board has about 100 MHz band width with 100 Ω input impedance, DC coupled. However, the **ATR19** in the standard version contains capacitors for AC-coupling of the inputs.
The **ATR19** is usually operated as a non-symmetric (single input) amplifier with 50 Ω impedance to ground, inverting (-) or non-inverting (+). This non-symmetric operation is the default mode for the use of a delay-line detector in combination with the (standard) **FT4/12/16TP** feedthrough and decoupling plugs.

The outputs of the **ATR19** allow verification of the signals after the first amplification stage on the **DLATR** board ("analog" signal) and of the NIM or ECL timing output signals. Amplification, trigger threshold and timing signal width can be adjusted by potentiometers (default) or externally by DC levels (0 to +5 V), the CFD "walk" adjust is automated (push-button) or pre-set (with **DLATR2**). Double-hit dead-time of the CFD-outputs is about 20 ns, depending on the input signal width. Since the amplifier inputs are internally not tolerant to both signal polarities (no bipolar amplification), it is required to feed signals into the inputs of corresponding polarity. Therefore, positive input signals (e.g. the signal from the MCP) must be connected via the inverting (-) input and negative signals must be connected via the non-inverting (+) input. To ensure proper input impedance of single polarity signals the other input of the internal amplifier should be terminated to ground (see Chapter 3.1).

* No mains power supply (neither from **RoentDek** units or others modules) should be placed near the **FAMP**, **ATR19** or **CFD** modules or the input signal cables to minimize the risk of EM-noise pickup.

The recommended readout version of the **RoentDek** delay-line detectors involves the **FT12(16)-TP** plug with internal signal transformers for the delay-line signals. For applications where only the single particle timing is of importance (e.g. with **DET40/75**) a **FT4TP**-type read-out in combination with the **ATR19-2** is recommended. The physical characteristics of the **ATR19-2** are described in Chapter 3.6.

When the **ATR19-6/8** is delivered, channel 1 and 2 are by default prepared for positive input polarity (inverting) and the other channels (used for the delay-line signals) for negative (non-inverting) signal polarity. (**ATR19-2** default: ch1 for positive input polarity (inverting) and ch2 for negative (non-inverting) signal polarity). If the voltages to the detector are supplied in the recommended way the signal from the MCP front or back contact (positive) has to be connected to ch1- or ch2- and the delay-line signals to ch3+ to ch6+ (or ch8+). In case of **DET40** and **ATR19-2:** the signal from the MCP front or back contact (positive) has to be connected to ch1- and/or the signal from the timing anode (negative) has to be connected to ch2. Changing these settings requires to open the **ATR19** module (see Chapter 3.5 and for **ATR19-2** also Chapter 3.6).

3.1 Signal inputs and amplification

The **ATR19-6/8** hosts three or four **DLATR** boards (one in case of **ATR19-2**). Each board has two independent channels for amplification and timing discrimination. Each differential amplifying stage has 100 Ω impedance (2x50 Ω to ground) and a selectable differential amplification gain between 20 and 100. The gain can be adjusted by a potentiometer ("poti") on each board and channel independently through holes in the top lid of the **ATR19-6/8** module. For **ATR19-2** the gain potis are found on side panel or fron panel, see Chapter 3.6.

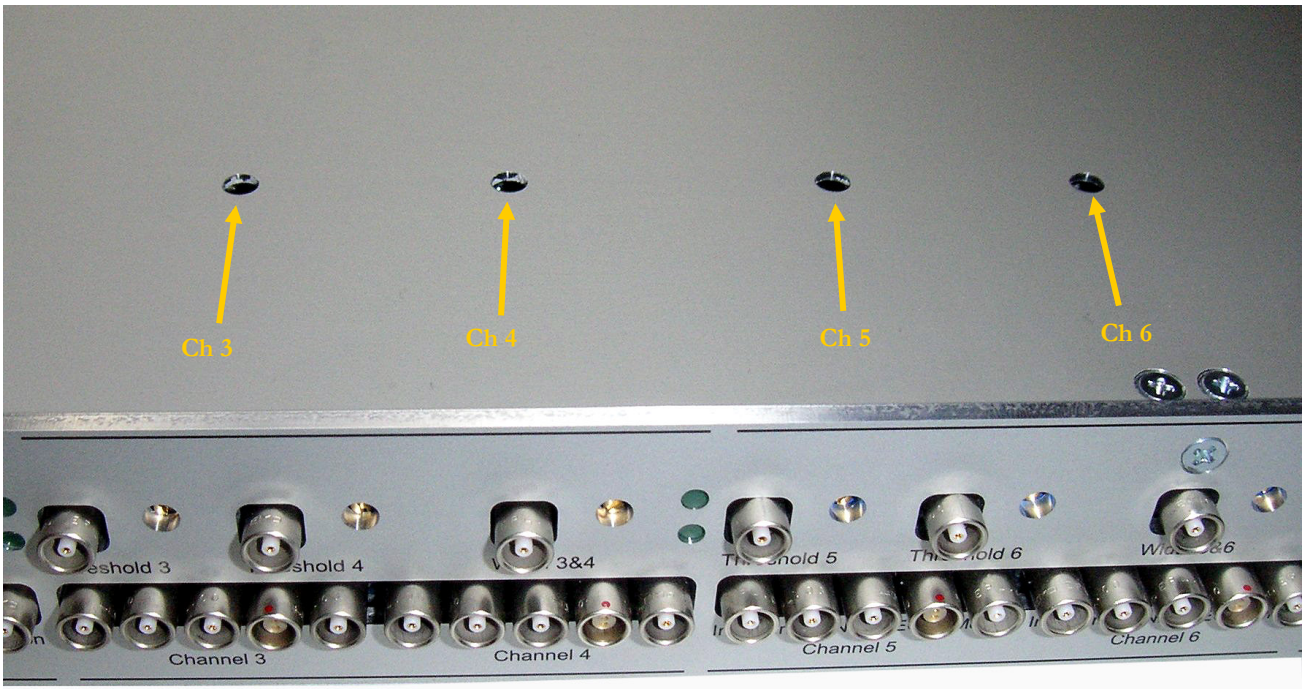


Figure 3.2: Top lid of ATR19-6/8 with holes to reach the gain potentiometers. Turning clockwise: amplifier gain is increased, turning counter clockwise: gain is decreased (for ATR19-2 refer to Chapter 3.6)

The input to each amplifier is provided AC-coupled via coaxial LEMO connectors with 50 Ω impedance. It is important to note the actual input settings for each individual channel inside the **ATR19**, i.e. the position of the termination jumpers JP5, JP6 (odd channel numbers of the ATR front panel) JP8 and JP9 (even channel numbers):

a) no jumpers: inputs + and – are active (differential) with 100 Ω impedance. Please observe the polarity
b) jumper on JP6/JP9: input – (inverting 50 Ω impedance to ground); can be used for positive input signals
c) jumper on JP5/JP8: input + (non-inverting 50 Ω impedance to ground); can be used for negative input signals

Default settings are: ch1 and ch2 as (b) and ch3 to ch8 as (c), for **ATR19-2**: ch1 as (b) and ch2 as (c) when used with a **DET** or both channels as (c) for read-out of a delay-line anode.

If you want to change these settings please refer to Chapter 3.5 and/or 3.6.

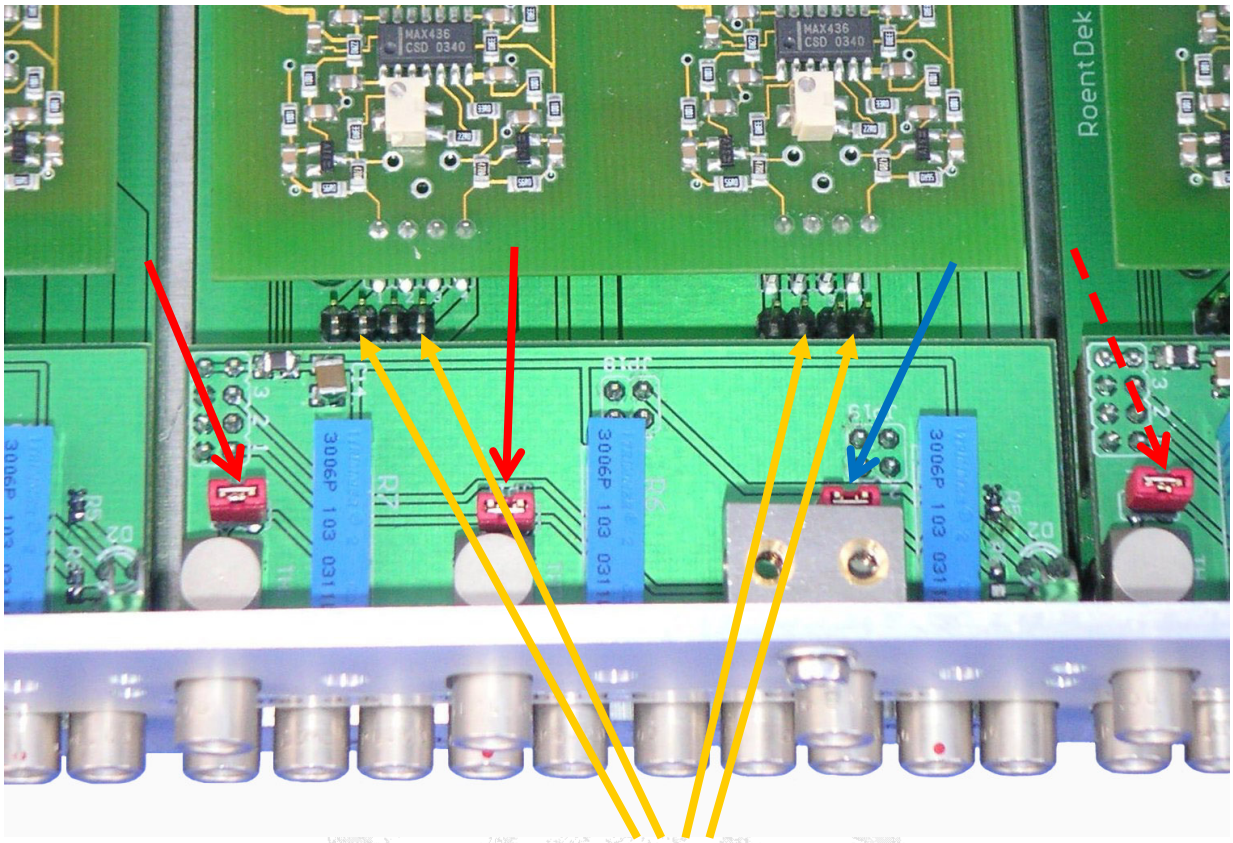


Figure 3.3: ATR19-6/8 with input settings for differential input (see yellow arrows: no input jumpers set). Red arrows point to jumpers that must be removed if threshold levels shall be controlled via external DC voltages rather than via front panel potentiometers, likewise for controlling output with of NIM/ECL signals (blue arrow).

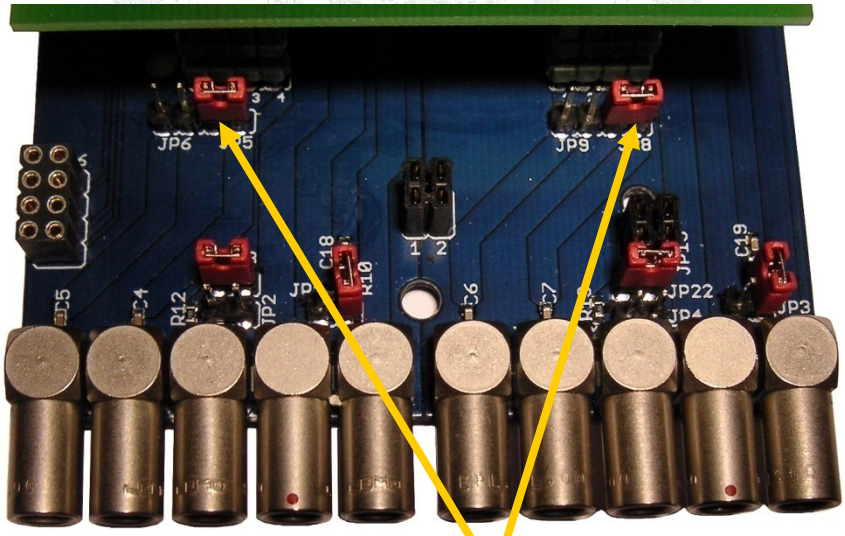


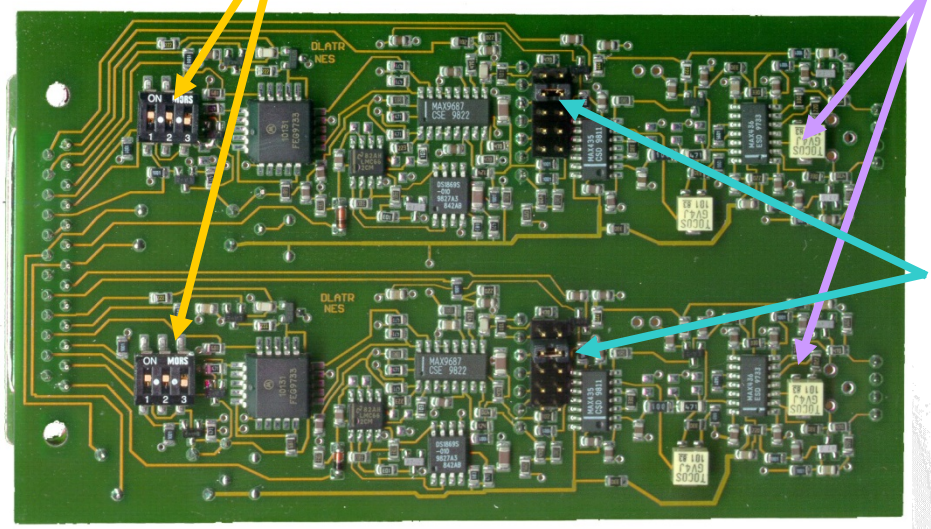
Figure 3.4: ATR19 base board with input jumper settings for signal input through the "+" LEMO input (50 Ω impedance to ground, non-inverting, for negative signal input). The level control board was removed here for better view.

3.2 The DLATR board

The **ATR19** module contains boards of type **DLATR**, which are occasionally updated in the circuit design without altering their function. Currently **DLATR+** or **DLATR2** boards are supplied (the latter for **ATR19-2b**). The board can easily be exchanged. To modify settings on the boards or exchange the boards please refer to Chapter 3.5. The amplification gain can be changed without opening the **ATR19** unit.

These 3 switches for each channel define the output level NIM or ECL (number 3 must always be „off“)

1: „on“ ECL, „off“ NIM
2: „on“ ECL, „off“ NIM



The marked potis, see purple arrows (2 kΩ for the **DLATR+**) adjust the amplification.

Higher resistance corresponds to lower amplification (not linear).

The marked jumpers, see blue arrows, define the internal CFD-delay. The figure shows the default position (8 ns for **DLATR** and 6 ns for **DLATR+**). From bottom to top: 2,4,6,8,10 ns

Figure 3.5: DLATR amplifier and constant fraction discriminator boards.

For **DLATR2**: the red arrows mark the walk potis and the test points (factory set to 12-14 mV)

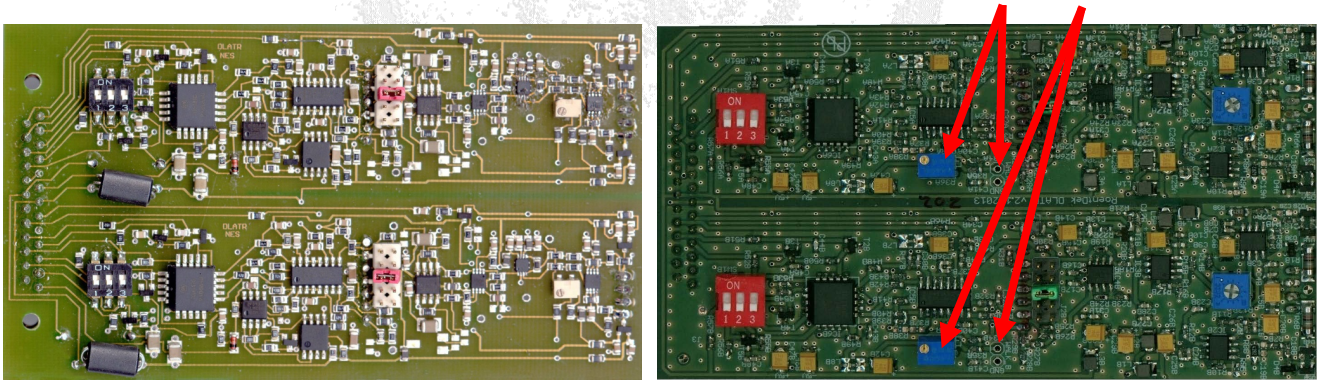


Figure 3.6: DLATR+ version (left) and DLATR2 (right)

If you insert a board make sure that the settings on the board are according to the requirements (e.g. signal level NIM or ECL). The switches have to be set according to the desired timing signals levels from the **ATR19** module.

Always switch off the power when inserting or retracting a DLATR board or changing settings on a board.

3.3 CFD controls and outputs

The **ATR19** has the following inputs, outputs and controls for each channel:

2 LEMO connectors In+ and In- for signal input (see Chapter 3.1)
3 LEMO connectors for signal outputs:

Mon analog output signal, i.e. the amplified signal before the CFD-stage.
ECL Timing signal output from the CFD circuit (differential ECL).
Only for the ECL version of the **ATR19**
NIM For the NIM version of the **ATR19**: NIM timing signal output from the CFD circuit.
For the ECL version of the **ATR19**: modified ECL- signal level from the CFD circuit for threshold control
2 LEMO connectors and potis for CFD threshold control
1 LEMO connector and poti for signal width control (for both channels of the same **DLATR** board)
2 LED for power verification of +5.2 V/-5.2 V for each **DLATR** board

Additionally there is a push button for the walk calibration of all channels (not for **ATR19-2b**), a power switch and reading points for the internal DC voltage supply to all boards on the **ATR19** front panel. The rear panel hosts the mains power input and selection switch (100-125 V or 200-250 V AC) and an alternative DC power input. Please refer to Chapter 3.5 if you want to use the DC power input.

Holes in the **ATR19-6/8** top lid allow access to the amplification gain potis of each channel (located at side or front panel for **ATR19-2**).

Figure 3.7: inputs, outputs and controls of the ATR19 (here version -6/8) for each internal DLATR board

The "Mon" output allows monitoring the noise level and analogue signal from the delay-line. This output shows the amplified signal according to the input signal and input settings (jumpers JP5, JP6, JP8 and JP9, see Chapter 3.1). For verifying the signal, the input of the oscilloscope must be 50 Ω coupled and the CFD output (ECL or NIM) should be connected to the TDC.

The "ECL" output (only for ECL version of the **ATR19**) provides the timing signal (differential ECL) from the CFD circuit for use with a TDC of according input requirement. The TDC input should provide -2 V via 50 Ω or from a similar passive differential ECL input.

The "NIM" output provides

for NIM version of the **ATR19**: the timing signal (standard NIM signal) from the CFD circuit for use with a TDC of according input requirement.
The signal can be verified on an oscilloscope (50 Ω coupling).
for ECL version of the **ATR19**: the modified timing signal from the CFD circuit (ECL -) for monitoring via an Oscilloscope: select AC coupling with large impedance (e.g. 1 MΩ)

The CFD circuit requires the setting of a threshold in order to discriminate noise from real signals. This threshold is typically set by a DC level of 0 to +5 V. This level can be set and controlled internally via the threshold poti for each channel (default) or by directly supplying this voltage through the corresponding LEMO input. For control via poti the LEMO output serves as measuring point for the actual threshold of the circuit, i.e. via an Ω meter. The jumpers (JP11 and JP12) on the level control board inside the **ATR19** (see Figure 3.3 and Chapter 3.5) enables the threshold control by the poti (default setting). If the jumper for a certain channel is removed the poti is disabled and the LEMO connector serves as input for the DC voltage from an external source. Please contact **RoentDek** for adequate remote DC level controls (e.g. via the **USB-IO2** module). The same scheme is applied for setting the width of the NIM/ECL output signal either via poti (default) or DC level (in absence of the respective jumper).

A DC voltage of +5 V corresponds to an internal threshold level of -100 mV on the amplified signal (as obtained from the "Mon" output). The ratio between DC voltage on the LEMO connector and the threshold is -50. Note that in case of **DLATR+** and **DLATR2** boards the pulse height indicated on the "Mon" output is only half of the real pulse height.

The width of the timing signal from the CFD is set by another DC voltage (0 to +5 V) which can likewise either be supplied by the corresponding poti and probed via the LEMO connector (JP13 set, default) or by directly supplying this DC voltage (JP13 off). Thus the width can be adjusted between 10 and about 100 ns. Note that there is only one control for both channels on each **DLATR** board.

If the LEDs next to each **DLATR** board in-/output connector group (on the right side) is not lit please verify the DC voltages on the reading points near the power switch on the front panel. If these are present and within the specified range (see Chapter 3.4) refer to Chapter 3.5 (opening the **ATR19**) and insure that the corresponding board is properly installed.
If the DC voltages on the reading points near the power switch on the front panel are not within specification verify the mains power or the external DC supply (see Chapter 3.4)

Before starting a measurement the "walk" of the CFD on all boards can be adjusted. This is generally not necessary and in case of the **DLATR2** the walk level is factory-set and the walk adjust button is disabled.

If you want to calibrate the walk (for all other boards) at the beginning of a measurement please follow these steps:

Switch off the high voltage on the detector
Verify that the noise level is low and that there are no signals from the CFD outputs.
Press the walk button for at least 1 second.
Wait at least 15 seconds for the automatic walk adjust

Then apply voltage to the detector and start/resume your measurement

3.4 Connecting and operating the ATR19

Before connecting the **ATR19** to any cable please ensure that the AC mains power from your socket complies with the setting of the switch on the rear panel (not for **ATR19-2**).
The setting "230" complies with a mains power of 200-250 V AC, 50-60 Hz, main fuse: 250 mA, time lag
The setting "115" complies with a mains power of 100-125 V AC, 50-60 Hz, main fuse: 500 mA or 630 mA, time lag

Warning: A wrong setting can lead to damage of the ATR19 and/or any connected appliances

After connecting the mains power through the standard mains cable input on the rear panel turn on the module with the switch on the front panel. Please verify that the DC voltages on the reading points on the front panel are between 5.5 V and 6.5 V - positive and negative - and that all LEDs are lit.

If the DC voltages are not present please check the mains voltage and the main fuse in the mains connector, replace the fuse if necessary. The main fuse is located above the mains input socket (see Chapter 3.8, not for **ATR19-2**). If main fuse, the switch position and the main power are properly set, you may follow the steps in Chapter 3.5 for opening the **ATR19** and verify the separate fuses for positive DC (1.6 A, swift) and negative DC (2.5 A, swift), replace fuses if necessary. The fuses are located on the voltage adapter board (see also Chapter 3.8, not for **ATR19-2**).

If you want to use the external ±6 V DC input (default for **ATR19-2**) instead of an internal mains power adapter please follow the steps in Chapter 3.5 for opening the **ATR19** and remove the internal cable connector from the mains adapter to the external input. If you have ordered the **ATR19** for use without AC mains adapter (e.g. **ATR19-2**), the cable is already connected in the correct way. For operating the **ATR19** DC voltages -6 V on pin 5 and +6 V on pin 8 (2 A each) are required, pin 1 and 2 must be grounded.*

The **ATR19** can also be supplied externally with ±5.2 V (or ±5 V) via the same connector. In this case the jumpers JP7 and JP10 (located under each **DLATR** board) have to be removed.

Attention: A few of the earliest **ATR19**, which have been delivered to customers, allow an external DC supply only with ±5.2 V (JP7 and JP10 removed). If in doubt please contact **RoentDek** to insure that your module can also be operated with ±6 V and JP7 and JP10 set.

* Adequate DC supply and cabling can be achieved from the **SPS1(b)** modules with a corresponding cable.

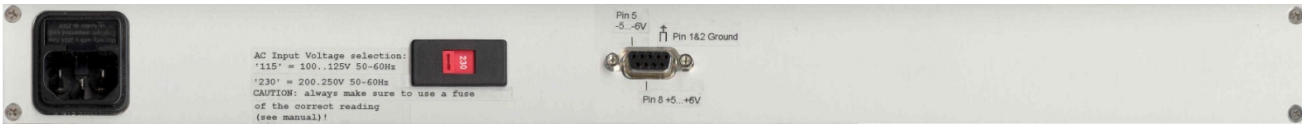


Figure 3.8: Rear panel of the ATR19 (for ATR19-2 see Chapter 3.6)

Before connecting the input cables to the LEMO connectors on the **ATR19** front panel make sure that the detector voltages are switched off and that you are aware of the input jumper settings for the respective channels and the active input connectors (see Chapter 3.1).

In the default versions of the **ATR19** (not **ATR19-2)** ch1 and ch2 (inverting) are reserved for the (positive) MCP signal input via the "In-" LEMO connector, while the other channels are non-inverting for signals from the delay line ends which shall be supplied through the "In+" LEMO connectors. The delay-line signals are negative if the U_{ref} and U_{sig} voltages are provided to the corresponding connectors on **FT12(16)-TP** as described in the detector manual. If these voltage inputs are interchanged, the signals from the delay-line will become positive and require connection via the "In-" inputs and changing the input jumpers inside the **ATR19** from their default settings (see Chapter 3.1).

When operating a **DET** with **ATR19-2(b)**: the signal from the MCP front or back contact (positive) has to be connected to ch1 In-. The signal from the timing anode (negative) has to be connected to ch2 In+.

Now you may also connect the "Mon", "ECL" and "NIM" outputs for signal verification and/or data acquisition with a TDC, depending on the **ATR19** version that you have obtained (see also Chapter 3.1).

If you operate the threshold and width controls of the **DLATR** boards via the potis (JP11, JP12, JP13 set) you may now connect the threshold and width LEMO connectors to an Ohm-meter for verification.

If you operate the threshold and/or signal width DC levels with external voltages (JP11, JP12, JP13 off) you must now connect the corresponding LEMO inputs. Before you can obtain output signals from the CFD output (ECL and/or NIM) these voltages must be set from your external DC source. The default values are 2 V and have to be finally adjusted during detector operation.

3.5 Opening the ATR19 module

You need to open the lid of the **ATR19** module **only** if

- you want to change the input impedance or inversion of an amplifier channel
- exchange a **DLATR** board
- switch between mains power supply to external DC power
- change the setting method for CFD signal width or threshold levels
- modify the CFD output level (ECL or NIM)

To open the top lid please follow these steps and for **ATR19-2** refer also to Chapter 3.6:

I. **ATR19-6/8**-channel version:
Switch off the ATR19 main power and retract any cables from the module.
Remove the 4 screws on the rear panel and the two screws on the top lid. Now the back panel is not fixed anymore to the rest of the housing but connectors in the rear panel are still wired to the main AC adapter board inside the **ATR19**.
Without pulling too much on the cables it is possible to retract the rear panel carefully for about 2 cm. Now the top lid can be retracted from its guide slots.
Retract the top lid
Fix the rear panel to the housing again. It is sufficient to fix the rear panel only provisionally by a couple of screws. When reinserting the screws make sure that they are entering the thread correctly.

Warning: when the lid is open you should not connect the mains cable to the socket. There is a severe risk of electroshock which might be fatal. The ATR19 shall not be operated with the lid open

II. All **ATR19** versions
Now you may change settings and jumper positions or exchange **DLATR** boards. For removing a **DLATR** board pull gently (simultaneously) on the upper and lower edges of the board. When you insert a board again first mate it to the input pins near the front panel then press the 25pin connector gently into the socket and insure that the connections are firm. Make sure that the settings on the **DLATR** board are correct and correspond to the **ATR19** version (ECL or NIM, see Chapter 3.2).

In order to change the settings for the signal level of timing outputs (ECL or NIM) it is required to remove the level control boards from the base board after loosening the front panel from the housing. This procedure and especially the re-assembly is complicated and not a recommended procedure for inexperienced users. If you want to change your **ATR19** module between ECL and NIM versions please contact **RoentDek**.

These are the following options for the signal output levels on the ECL and NIM output connectors:

Standard NIM: JP1/JP3 and JP2/JP4 set, JP22/JP23 open (as in Figure 3.4)

The timing output from the CFD is present on the "NIM" LEMO connector as standard NIM level.

If JP1/JP3 is left open the CFD output signals will also be present on the upper pin (red dot) of the "ECL" LEMO connector as the positive ECL+ level. Please inquire before you intend to use this option.

Standard ECL: JP22/JP23 set, JP1/JP3 and JP2/JP4 open

The timing output from the CFD is present on the "ECL" LEMO connector as standard (differential) ECL levels. The ECL+ level is found at the pin near the red dot and the ECL- at the lower pin. Additionally, the ECL- level is supplied via a 50 Ω resistor in line to the "NIM" LEMO connector for control (see Chapter 3.3)

If JP2/JP4 is set and JP22/JP23 is left open the ECL- level is directly present on the "NIM" LEMO connector without in-line resistor. Please inquire before you intend to use this option.

If you change the settings of your **ATR19** between ECL and NIM you must also change the settings on the **DLATR** boards (see Chapter 3.2).

To close the top lid (**ATR19-**6/8-channel version), take off the rear panel again. Insert the top lid into the guiding slots and fix the rear panel tight with the screws. For **ATR19-2** refer to Chapter 3.6.

3.6 The ATR19-2(b) module

The **ATR19-2(b)** module is a 2-channel (1 **DLATR** board) version of the above-described **ATR19** module series. It measures 3HU (19" rack height units) and has no internal mains adapter.

The **ATR19-2b** can be operated with the supplied 12 V mains adapter, which can supply several units (at least 4) chained in series via rear panel connectors. For operation of the older version **ATR19-2**, ±6 V DC (600 mA) need to be supplied via the rear panel connector, e.g. from the **SPS1(b)**.

All other functions/settings are mostly identical† to the **ATR19-6** or **ATR19-8** module versions. The latest version of **ATR19-2b** allows access to the gain adjustment via potentiometers on the front panel.

To open the module remove the screws on the front and rear panel which fix the right side panel (the one with holes). Now you can remove the side panel and have access to the **DLATR** board inside. For complete disassembly and full access to all parts

† For the **ATR19-2b** it is not necessary placing jumpers at JP5/JP6 or JP8/JP9. Both inputs *IN1* and *IN2* can be used according to the polarity of the input signal *(IN1* for negative, *IN2* for positive signals).

remove also the remaining screws on front and rear panel.

Figure 3.9: ATR19-2b module

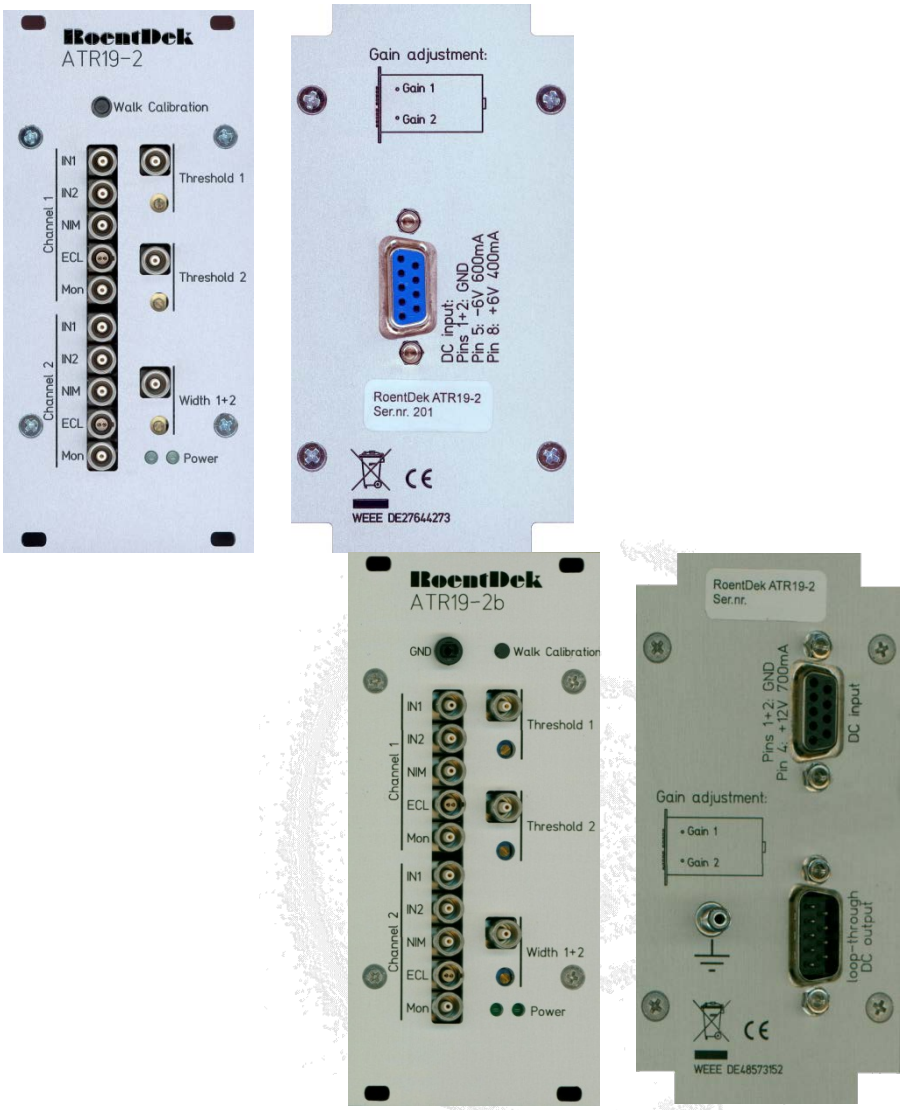


Figure 3.10: Front and rear panel of the ATR19-2 (left) and ATR19-2b (right)

3.7 Final Adjustment for detector operation

The **ATR19** units were specifically designed for the read-out of **RoentDek** delay-line detectors (**ATR19-6** for **DLD**, **ATR19-8** for HEX) and timing detectors (**ATR19-2**). The **ATR19-2** can also be used for the read-out of one delay-line layer.
If the voltages to the detector are supplied in the recommended way the signal from the MCP front or back contact (positive) has to be connected to ch1- or ch2- and the delay-line signals to ch3+ to ch6+ (or to ch8+). In case of **DET40/75** and **ATR19-2**: the signal from the MCP front or back contact (positive) has to be connected to ch1- and/or the signal from the timing anode (negative) has to be connected to ch2.
During the initial start-up procedure and whenever there are doubts about the high voltage robustness of the detector hardware, only the MCP signal should be connected for verifying the general detector (MCP) function. After an initial start-up procedure you have verified signals and the noise level from the detector. Assuming all wire connections are correct and all detector potentials are applied you should see similarly shaped analogue output signals on MCP front/back and the delay-line (monitor outputs). The outputs from the delay line should have similar signal heights. If not, the amplification factors on the DLATR boards should be adjusted (see Figure 3.2).

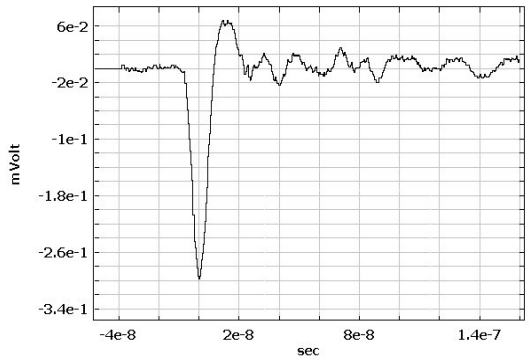


Figure 3.11: Typical amplified pulse shape of the MCP as obtained from the ATR19 analogue monitor output.

The analogue signal height on MCP back or front (channel 1 or 2) linearly corresponds to the charge of the electron cloud delivered from the MCP for a respective particle. As long as the output pulse height is smaller than 400 mV (negative polarity) the shape of the pulses resembles the input signals that enter the constant fraction stage. For older **DLATR** boards the analogue output saturates at this value, however, internally (at the CFD input stage on board) the pulse height can be higher and is still linear. For normal noise levels below 50 mV sufficient imaging results are obtained if the pulse heights distribution has a mean value of 300 mV. The lowest pulse height should still be higher than the noise level. To increase the pulse height one can increase the MCP bias (not exceeding the maximum recommended value!) or the amplifier gain. If you increase the amplifier gain please be aware that the noise level will increases proportionally to the amplification factor. The signal-to-noise ratio, limiting detector performance, can only be improved be increasing MCP gain (which may require reducing amp gain for avoiding saturation effects and non-linear amplification).

If the analogue outputs are satisfactorily, one can check the corresponding timing (CFD) outputs on the sockets "NIM" or "ECL". If your module is set to NIM-output levels you can directly verify the signals on an oscilloscope (coax input, 50Ω terminated). For the ECL output setting the presence of signals can be probed likewise on the NIM output with an oscilloscope (but with at least 1MΩ input impedance). Note that this may disturb the signal from the ECL output). Now the thresholds on all channels can be adjusted, ideally so that even the smallest pulse heights from particle/photon triggered MCP charge cloud are above the threshold but noise is still fully discriminated (typical threshold level 1.5x - 2x higher than the continuous noise level). Figure 3.12 shows such a typical case. It should be noted that it may be beneficial to allow occasional noise triggers in order to safely detect also the smallest real signals and not to "lose" counts. This will not lead to false data because if they do not appear on all signal chains or if such random counts can be dismissed in coincidence-triggered measurements. Such signals will either not be processed by the data acquisition or can easily be sorted out later during data analysis (see below).

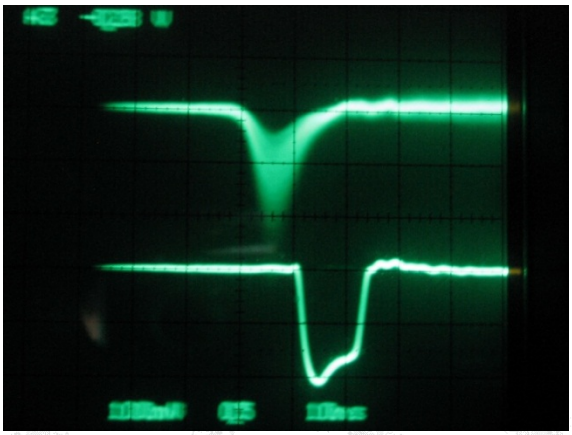


Figure 3.12: Typical (analogue) oscilloscope screen output showing delay-line signals from a DLATR+ board: analogue signals (monitor output) on upper trace and the correlated CFD outputs (NIM) on the lower trace. Both traces are triggered by the NIM signal. The pulse height distribution of the analogue signals can be seen and also the effect of the threshold setting on the registered events (cut-off of smaller signals not being registered).

However, one should avoid a too-low threshold setting which may cause a so-called "pre-trigger" operation mode of the CFD circuit. In this mode the CFD threshold will not block off signals that have been slightly distorted by noise in a way that the CFD circuit can function normally, see Figure 3.13. If the pre-trigger signal is registered a false time will be measured. For delay-line signals this can be recognized in a false time sum for this detected particle / photon on the respective layer and the event can be dismissed by software. However this may lead to non-linear imaging and timing response on the detector.

If thresholds are set to a very low value it can be of advantage to mix the delay-line outputs between channels so that signals from the same delay-line layer (i.e. from x1 and x2 outputs) are not processed on the same internal board, i.e. on those neighbouring channels that share a width potentiometer. Otherwise inter-channel cross talk is more likely to happen.

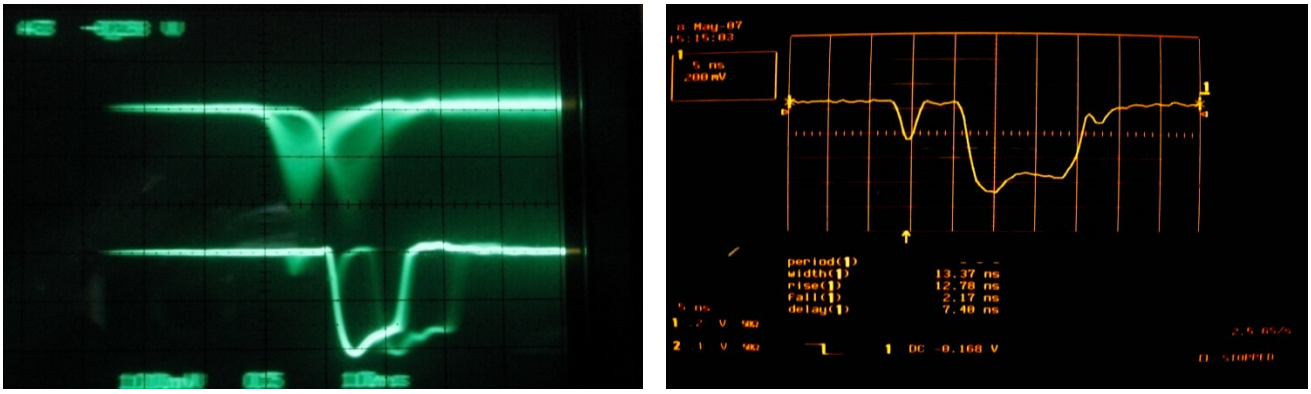


Figure 3.13: Signal traces as in Figure 3.12, but with low threshold setting very close to the noise level (left). Pre-triggered signals are present. The right picture shows the CFD output of an erroneous pre-triggered event.

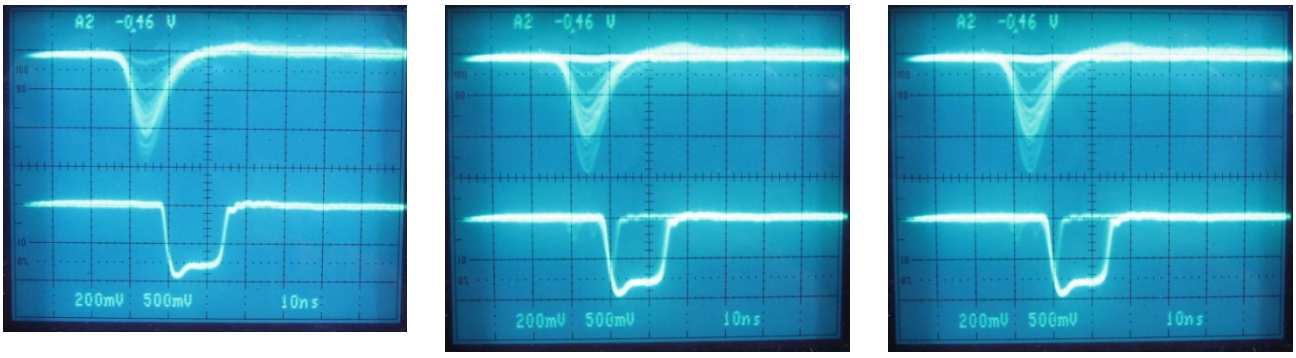


Figure 3.14: Overview of ATR19 signal outputs for low threshold settings, triggered on the CFD signal.

Figure 3.14 shows signals at low threshold values. Ideally, the threshold should be set so low that all valid input signals produce a NIM-output from the CFD stage (left image) but high enough to exclude noise triggers (as in the middle image) and pre-triggers (as in the right image). The spurious per-trigger events can be identified by a small signal appearing occasionally just before the "main" NIM signal on the CFD output line.

If a RoentDek delay-line detector is used the presence of such events can be clearly observed in the time sum spectrum during data acquisition, see Figure 3.15. Ideally, the time sum on each layer consists only of one narrow peak with few ns width (lower pictures left side). Pre-trigger events contribute a more or less continuous "background" of falsely timed signals (lower pictures right side). It should be noted, however, that also a too high threshold level on the CFDs for the delay-line leads to a "non-perfect" time sum spectrum.

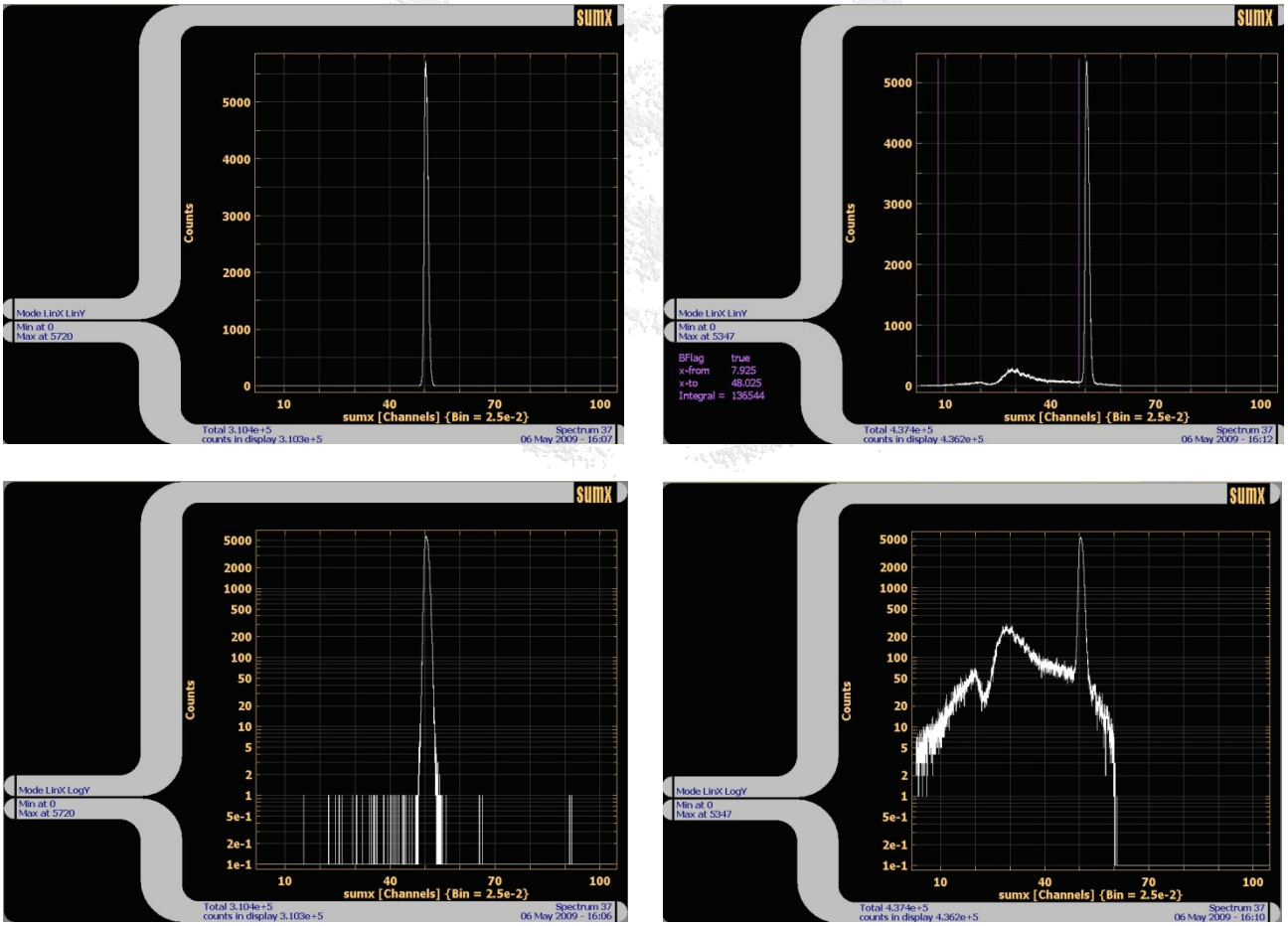


Figure 3.15: Time sum spectra from a delay-line anode for different threshold setting. Left: clean spectrum, right: contribution of noise and pre-trigger signals can be seen. Setting a software gate on the time sum peak may still produce results with a decent imaging performance.

It is not recommended to simply remove pre-trigger events by setting a narrow software window in the time sum spectra because these pre-trigger events are not uniformly distributed across the active area of a delay line detector, see Figure 3.16.

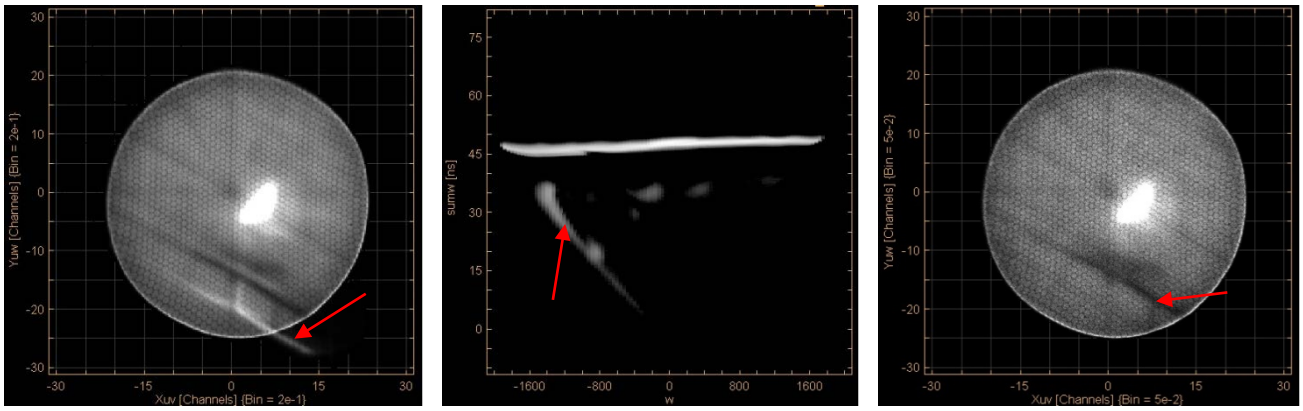


Figure 3.16: Typical image artefact caused by pre-trigger events (left picture). These events may appear only on certain parts of the detector (see red arrow). Here, thresholds of the channels for the w-layer were set too low, causing image artefacts. If the time sum is plotted as function of position (middle picture) the localized contribution of pre-trigger events is revealed. Setting a narrow time sum gate can remove the pre-trigger events but the image artefact (missing data) remains, see right picture.

3.8 Troubleshooting the ATR19's internal mains power supply

This chapter shall assist you in fixing problems with the **ATR19** (not **ATR19-2**) internal mains supply, which is very similar to the **SPS1**. It describes procedures to verify the internal power supply and how to change fuses in case of problems. A problem with the internal power supply is indicated if some of the green LED in the front panel are not lid or the voltages in the front panel test points are not between 5.5 and 6.5 V, both polarities. A FAQ (Frequently Asked Questions) list on the **ATR19** and its functions is continuously updated. Please refer to our WEB site for updates of this manual.

1) Turn on the **ATR19**. **Check if the green power switch is lit** (the switch illumination might be very dim if the **ATR19** is operated with 100-115 VAC).

   If not: check the power connection. Check the fuse at the back panel of the ATR19 (fuse holder is integrated into the mains plug socket, see picture below) and replace when necessary. Only use fuses of the following readings:

   250V 630 mA T when operated at 100 VAC
   250V 500 mA T when operated at 115 VAC
   250V 315 mA T when operated at 200 VAC
   250V 250 mA T when operated at 230 VAC
   (T = (German:) träge = slow blow = time lag)

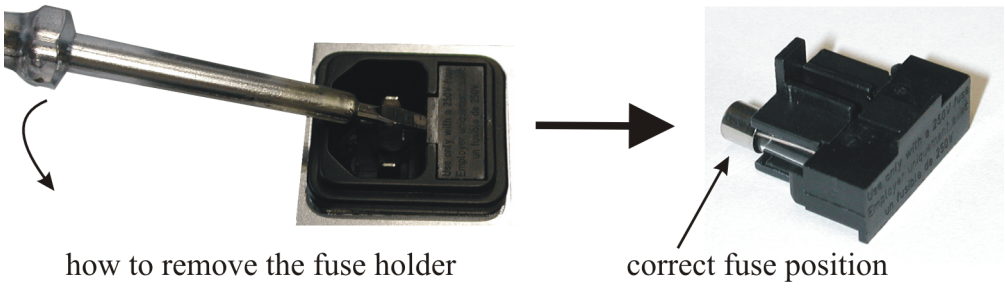


Figure 3.17: Opening the fuse holder

   If the problem persists please follow steps 2) to 9).

2) Remove the power cord and all other cables connected to the **ATR19**. Open the **ATR19** case. Check that all internal cables are correctly fixed in the terminals (yellow arrows in the picture below).

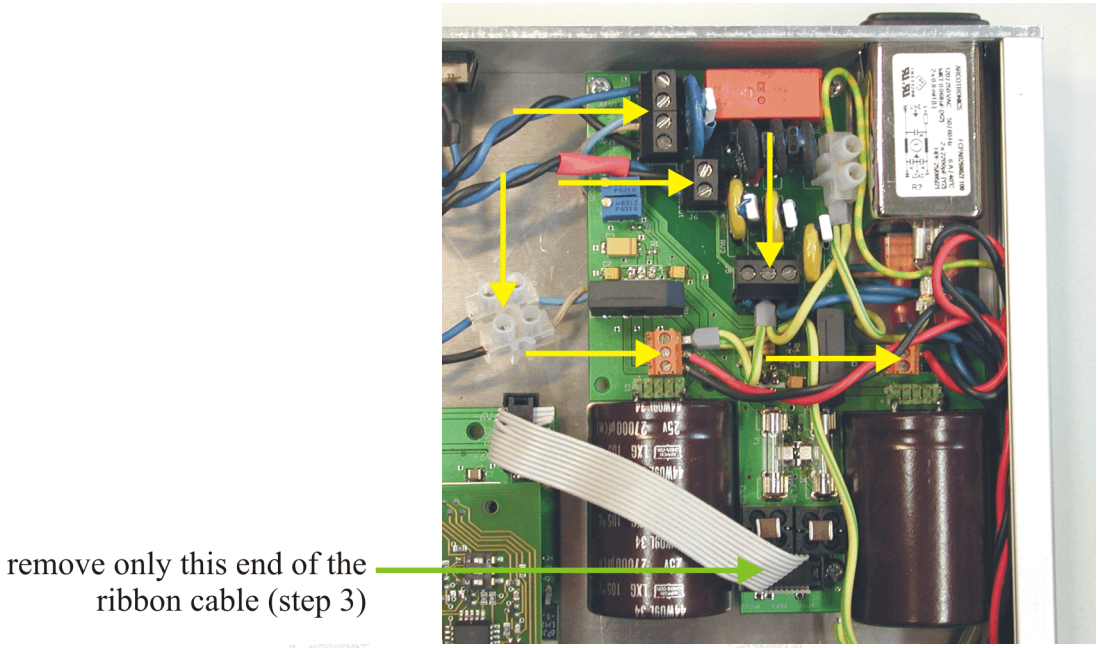


Figure 3.18: Remove the ribbon cable from the power supply

3) Remove the ribbon cable from the power supply (green arrow in the picture above). Make sure not to remove the other end of the ribbon cable. This will ensure that you will not invert polarity when reconnecting the cable later.

4) Check the output fuses (see picture below). If broken replace with fuses of the following readings:

F1: 250 V 1.6 A F
F2: 250 V 2.5 A F
(F = (German:) flink = fast acting)

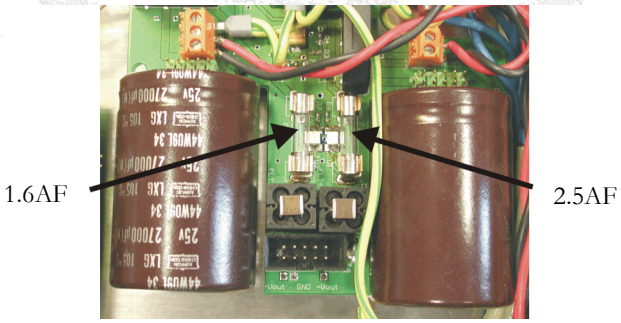


Figure 3.19: Output fuses

Use an ohmmeter to check that there are no short circuits between $+V_{out}$ and GND resp. $-V_{out}$ and GND (see picture below).

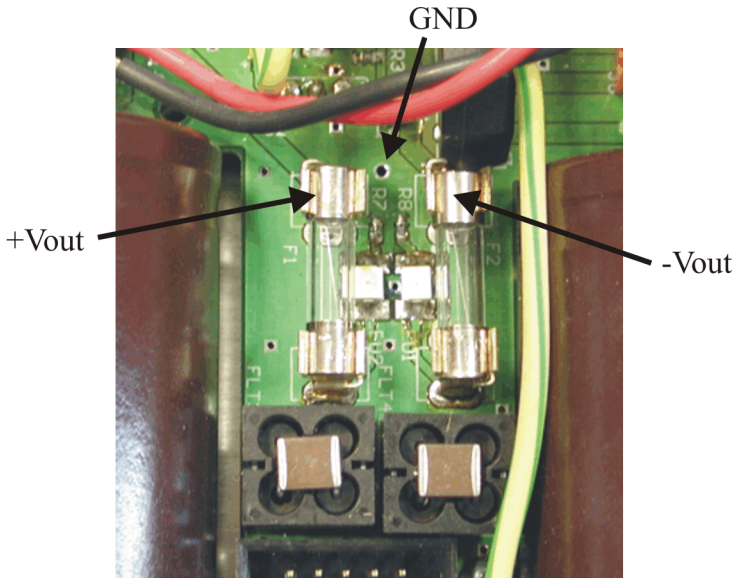


Figure 3.20: Voltages near the output fuses

5) Reconnect the ribbon cable to the power supply. Make sure that both connectors of the ribbon cable are firmly pressed in place.

6) Repeat step 4).

7) Check all the LEDs at the front panel (see picture below). Make sure that none of their pins touch each other or touch any other components of the **ATR19** since this might cause short-circuits. If necessary, bend the pins in order to remove any false contacts.

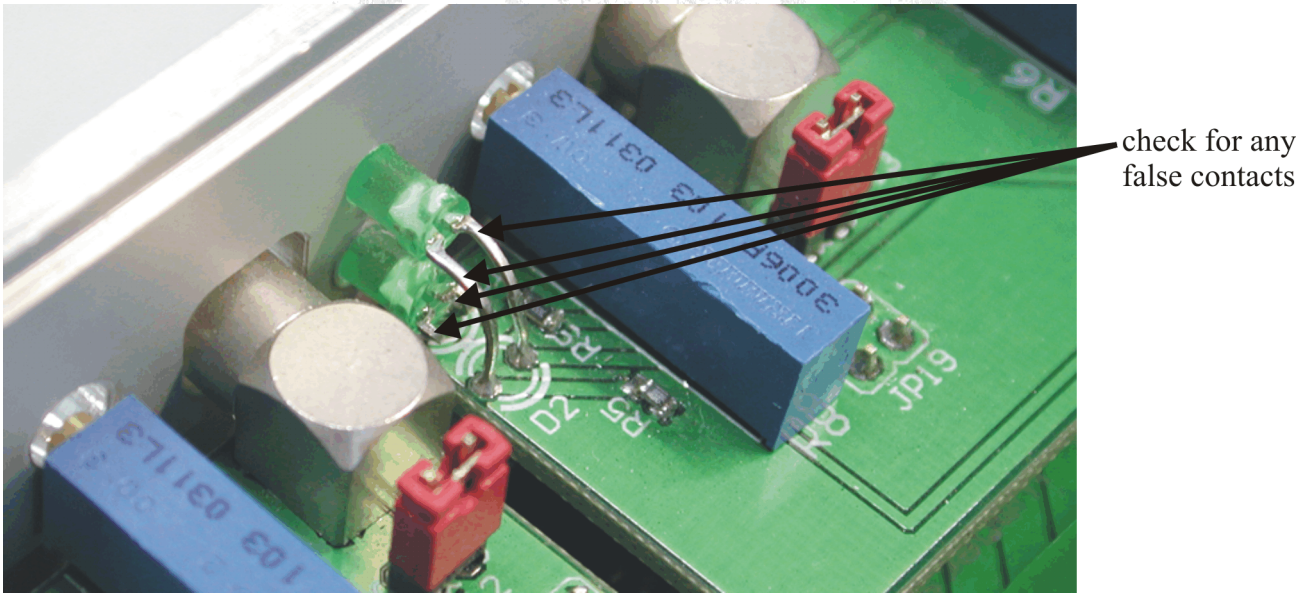


Figure 3.21: LEDs at the front panel

8) Close the casing of the **ATR19**.

9) Restore the power connection and check if the problem has been solved. If not, repeat the steps above. If the failure persists, contact **RoentDek** for further assistance.

List of Figures

List of Tables

NO TABLE OF FIGURES ENTRIES FOUND.